

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Applicant:** Jaroslav Hyneccek

**Art. Unit:** 3663

**Serial No.:** 10/633,993

**Examiner:** Johannes P. Mondt

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**Docket:** TI-36483

**For:** Clocked Barrier Virtual Phase FF, FT, and FIT CCD Image Sensors with Charge Multiplication Readout

Commissioner for Patents  
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Dear Sir:

This is Appellant's Amended Summary of Claimed Subject Matter in connection with the above-identified application in response to the Notification of Non-Compliant Appeal Brief mailed **September 25, 2007**.

## SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 10, line 16 to page 14, line 2, provides a concise explanation of the invention defined in independent claim 11.

The first clocked gate in claim 11 is gate electrode 307 in Figure 3 and gate electrode 409 in Figure 4.

The field plate in claim 11 is field plate gates 305 in Figure 3 and field plate gates 407 in Figure 4.

The second clocked gate in claim 11 is gate electrode 309 in Figure 3 and gate electrode 410 in Figure 4.

Generation of unwanted clock induced dark current is eliminated in the sensor serial and charge multiplying register pixels by incorporating new CCD register design, whose simplified cross section is shown in drawing 300 in FIG. 3. P-type doped silicon substrate 301 has n-type doped buried layer 302 near its surface. Oxide layer 304 on top of the silicon surface separates substrate 301 from poly-silicon gates 305, 307, and 309. The first deposited layer of poly-silicon forms field plate gates 305, which are connected using metal wiring 306 to bias terminal. The second poly-silicon layer, separated from the first one by an oxide dielectric layer, forms separate and independently biased gate electrodes 307 and 309, which are also connected using respective metal wirings 308 and 310 to corresponding bias terminals. Directionality of charge transfer is established by placing suitable barrier implants 303 under a portion of each gate 307 and 309. There are other possibilities and other implant combinations that can create the desired potential profile within each pixel, which are well known to those skilled in the art, and therefore do need to be described here in any further detail. The above described gate structure, after partial depletion of mobile charge, creates potential profile in each pixel that is described by segments 314, 315, 311, 312, and 313. In this example gate 307 is biased in its high biasing level and gate 309 in its low biasing level. Circles 317 indicate the electron charge transfer within the pixel. It is important to note that field plate gate 305 is

biased at a DC biasing level and is not clocked. Introducing field plate into the gate structure has two advantages. The field plate is used to create a suitable potential profile that confines charge in the direction perpendicular to the plane of the drawing without the necessity for heavily doped p+ channel stops. This eliminates the source of unwanted clocking induced dark current caused by impact ionization within such channel stops. The second advantage is a better control of potential profile when this pixel structure is used in charge multiplying registers and the charge-multiplying gate needs to be biased to high biasing levels necessary for the onset of electron multiplication.

For a better understanding of design details of the serial register of present invention, simplified drawing 400 of an example of one possible layout embodiment is shown in FIG. 4. Drawing 400 also shows the details of the interface region between the CCD memory area and serial register. The memory area consists of CCD columns separated by p+ doped channel stops 401. For simplicity only a conventional VP CCD gate structure 403 is shown with barrier region 405 and well region 404. However, the new CB VP CCD structure, shown in drawing 200, can easily be substituted here as is clear to all those skilled in the art. Gate 403 interfaces with virtual well region 402 and virtual barrier region 406 that further interfaces with field plate region 407 of the serial register. Field plate region 407, formed from the first poly-silicon layer, has openings 415 and notches 413 that are overlaid by the second poly-silicon layer, which forms gates 409 and 410. Metal wirings 408, 411, and 412 serve as interconnects between gates, the field plate, and the biasing terminals. Charge flow directionality is established by implanting barrier regions 414 and 416 under gates 409 and 410. Charge that is transferred from memory area into the serial register flows from Virtual Barrier region 406 under field plate region 422 and further under gate 409. Charge is confined to stay in these regions by suitable potential barrier forming implants 417 and 418 that have replaced the traditional p+ channel stops used in conventional designs. It is thus apparent that gates 409 and 410, which transport charge in serial register do not overlap any p+ channel stop anywhere. This eliminates generation of spurious clocking induced dark current even for high biases required for the onset of charge multiplication. An important feature introduced in this design is the serial register blooming protection. This is accomplished

by incorporating anti-blooming barrier implants 421 under gates 409. When a large amount of charge accumulates under these gates, either from excessive charge multiplication in charge multiplying sections of the register or from summing of several lines of data transferred from the memory into the register, excess charge can harmlessly overflow into drain 419 without corrupting charge signal under neighboring gates 410. Overflow charge collecting drain 419 is connected to biasing terminal by wiring 420. The drain interfaces with active device border 423. It is also apparent to those skilled in the art that it is possible to eliminate drain 419 and replace it with another complete serial register structure described above and transfer overflow charge through another charge confining region, similar to region 422, to this register. Several registers can thus be placed next to each other, their gates ganged together in parallel, and overflow charge transferred from one to the next before the final overflow charge is drained out from the structure. This design option is important for constructing devices that can handle high Dynamic Range signals.

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